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TITLE OF THE INVENTION

A SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a semiconductor device and a method of manufacturing the device, in particular, a structure of isolation in a semiconductor device.

DISCUSSION OF BACKGROUND

In accordance with development of integrated circuit design and process technologies, it becomes possible to manufacture an integrated circuit (IC) in which a memory element of high density and an operational circuit of high density are equipped in a single chip, whereby microminiaturization and high efficiency of a device is increasingly proceeded. Particularly, a highly integrated logic circuit (hereinbelow, referred to as logic circuit) represented by a microprocessing unit (MPU) and a dynamic random access memory (DRAM) are formed in a single chip to thereby form a logic consolidating dynamic random access memory. In producing such a logic consolidating DRAM, it is necessary to fabricate a plurality of MOS elements, respectively having different purposes, in the single chip. Therefore, the production is controlled to obtain desired

transistor characteristics in correspondence with these purposes by changing the film thickness of a gate oxide film.

In such a semiconductor device, isolation for insulating elements is preferably attained by trench isolation, which can extremely reduce an occupying area and a parasitic capacitance in comparison with the other isolation for insulating. Such trench isolation is effective for high integration and high speed. The trench isolation is formed by embedding a silicon oxide film in a groove by a chemical vapor deposition (CVD) method and etching its surface to leave the silicon oxide film only in the groove after forming the groove on a surface of a semiconductor substrate to be an isolation area, wherein the CVD method is suitable for microminiaturization in comparison with a case that a separation film is formed by thermal oxidation because it can restrict a decrement of active region caused by bird's beaks and control the shape of the trench isolation.

Figure 20 is a cross-sectional view for showing elements of the conventional semiconductor device, in which a DRAM memory cell and a logic circuit are formed on a single semiconductor substrate. In Figure 20, numerical reference 101 designates a semiconductor substrate; numerical reference 102 designates a groove, numerical references 103 and 104 designate silicon oxide

films; numerical references 1051 and 1052 designate gate oxide films; numerical reference 106 designates a polysilicon layer; numerical references 1061 and 1062 designate inter-layer insulating films; numerical reference 107 designates a metallic silicide layer; numerical reference 108 designates a side wall; numerical reference 109 designates a gate electrode; numerical references 1010 through 1013 designate source/drain areas; numerical reference 1018 designates a storage node; numerical reference 1019 designates a capacitor insulating film; numerical reference 1020 designates a cell plate; and numerical reference 1022 designates a capacitor composed of the storage node 1018, the capacitor insulating film 1019, and the cell plate 1020. Trench isolation is composed of the groove 102, and the silicon oxide film 103 and 104, by which active regions are separated. The gate electrode 109 is composed of the polysilicon layer 106, the metallic silicide layer 107, and so on.

The source/drain layer 1011 and the gate electrode 109 are horizontally overlap each other and interposed by a gate oxide film 1051. When a degree of microminiaturization is enhanced, the proportion of the width of overlapping to a memory cell becomes large. Therefore, for example in a case of nMOS, a high electric field was generated on a surface of the source/drain area 1011 and a leakage current caused by band to band

tunneling (BTBT) was sometimes generated between the capacitor 1022 and the semiconductor substrate 101 in reference X of Figure 20 when a voltage higher than that to the gate electrode 109 was applied to the source/drain area 1011. Non-flow of the leakage current is the most important characteristic in DRAM memory cells. Because when the leakage current is generated, refresh characteristics are deteriorated to cause problems in aspects of power consumption and reliability, it is necessary to reduce a mutual influence between the gate electrode 109 and the source/drain area 1011 by making the thickness of gate oxide film 1051 about 7 through 10 nm when the gate length L_1 of the DRAM memory cell is about 0.2 μm.

A high-speed transistor having a great driving capability is required in portions other than the memory cell such as a logic element and a peripheral circuit of DRAM, wherein it is the most important characteristic that an on-current sufficiently flows. Thus, gate oxide films 1052 of transistors in a logic circuit were formed to be thinner than gate oxide films 1051 of transistors in a DRAM memory cell by 3 nm in a case that the gate length L_2 was about 0.2 μm to suppress a leakage current in a memory cell and to enhance a driving capability in portions other than the memory cell.

However, the conventional device had problems that when gate oxide films having different film thicknesses

were formed on a single semiconductor substrate, silicon oxide films embedded in insides of grooves formed on the semiconductor substrate to serve as trench isolation was dropped into the grooves along the side walls of the grooves at positions adjacent to active regions in a portion other than the memory cell.

Figure 21 is a cross-sectional view for showing an element of the conventional semiconductor device which enlarges reference Y in Figure 20. As shown, although the silicon oxide film 104 embedded in an inside of the groove 2 is properly formed in the memory cell, the silicon oxide film 104 is dropped along an interface between the active region and the groove 102 in the logic circuit.

Figures 22 through 27 are cross-sectional views for illustrating steps of manufacturing the conventional semiconductor device, wherein numerical reference 1031 designates a silicon oxide film and numerical reference 1021 designates a silicon nitride film. At first, the silicon oxide film 1031 and the silicon nitride film 1021 are formed on a surface of a semiconductor substrate 101; the silicon nitride film 1021 is patterned to have openings for grooves 102 using a photoresist mask (not shown); and the grooves 102 are formed using the patterned silicon nitride film 1021 as a mask. Figure 22 is a cross-sectional view of the semiconductor device after this step.

In Figure 23, numerical references 103 and 104 are silicon oxide films. After forming the silicon oxide film 103 in the grooves 102 by thermal oxidation, the silicon oxide film 104 is embedded in the grooves 102 by a CVD method. Figure 23 is a cross-sectional view of the semiconductor device after this step. Finally, a surface of the silicon oxide film 104 is planarized by a chemical mechanical polishing (CMP), the silicon nitride film 1021 and the silicon oxide film 1031 are removed, whereby trench isolation is completed. Figure 24 is a cross-sectional view after this step.

In Figure 25, numerical reference 1053 designates a gate oxide film, and numerical reference 1042 designates a resist pattern. After forming the gate oxide film 1053 having a thickness of about 3 through 6 nm on a whole surface by thermal oxidation, the resist pattern 1042 for covering an active region of a DRAM memory cell is formed; and a part of the gate oxide film 1053 on a surface of an active region of the logic circuit is removed using the resist pattern 1042 as a mask. Figure 25 is a cross-sectional view of the semiconductor device after this step. As illustrated, because the part of the gate oxide film 1053 in the logic circuit is removed and the other part of the gate oxide film 1053 in the memory cell is left, the silicon oxide film 104 is shaped to drop into the grooves along an interface between the gate oxide film 1053 and the grooves 102 in the logic circuit.

After removing the resist pattern 1042, a gate oxide film 1052 having a thickness of about 4 through 7 nm is formed again on a whole surface by thermal oxidation; and gate electrodes 109 are formed. Figure 26 is a cross-sectional view for illustrating element of the semiconductor device after this step.

Thereafter, a side wall 108, source/drain areas 1010 and 1011, source/drain areas 1012 and 1013, an inter-layer insulating film 1061, a contact hole 1016, a wire 1017, an inter-layer insulating film 1062, a contact hole 23, a storage node 1018, a capacitor insulating film 1019, and a cell plate 1020 are formed thereon, whereby the semiconductor device shown in Figure 20 is fabricated.

Figure 27 is a cross-sectional view taken along a line Z-Z of Figure 26. A drop 190 shown in Figure 27 may be produced along all interfaces between the grooves 102 and the gate oxide film 1052 in the logic circuit, wherein when the silicon oxide film 104 was dropped, an inverse narrow channel effect occurred by concentration of electric fields in an end of the active region under the gate electrode, whereby there was a problem that a threshold voltage was decreased.

Conventional techniques are described in JP-A-3-99430, in which a method of manufacturing a semiconductor device having a CMOS structure for conducting ion channeling by injecting ions using a silicon oxide film

and a silicon nitride film as masks, and JP-A-9-74072, in which a method of manufacturing a semiconductor device having a CMOS structure for injecting to a well and injecting ions into a gate electrode using a single mask, wherein these techniques are for the semiconductor devices having uniform film thicknesses of gate oxide films.

SUMMARY OF THE INVENTION

It is an object of the present invention to solve the above mentioned problems inherent in the conventional technique and to provide a semiconductor device in which a silicon oxide film at a position along an edge of a groove is not dropped; shapes of end portions of active regions in contact with trench isolation can be made substantially the same; properties of transistors are not affected by the shapes of the active regions; and miniaturization of a chip is realized with maintaining preferable properties of elements, even though the transistors having different film thicknesses of gate oxide films are included in a DRAM memory cell, a logic circuit and so on in a single conductor substrate, and to provide a method of manufacturing such a semiconductor device.

According to the first aspect of the present invention, there is provided a semiconductor device comprising: grooves formed on a main surface of a semiconductor substrate, a silicon oxide film embedded in

insides of the grooves, a first active region disposed on a first portion of the main surface of the semiconductor substrate interposed between the grooves, first field effect transistors having a first gate oxide film formed on the main surface of the first active region, a second active region having the same shapes of end portions as those of the first active region, disposed between the grooves in a second portion of the main surface of the semiconductor substrate, second field effect transistors having a second gate oxide film of a film thickness different from that of the first gate oxide film formed on the main surface of the second active region, whereby a part of the silicon oxide film along an edge of a groove is not dropped even though the gate oxide films respectively having different film thicknesses are formed on surfaces of a plurality of active regions in a single chip; and transistor properties are not affected by shapes of the active regions because shapes of end portions of the active regions in contact with trench isolation are made substantially the same.

According to a second aspect of the present invention, there is provided a semiconductor device, wherein: the widths of the grooves interposing the first active region and the second active region are the same; and the heights from the bottom surfaces of the grooves to surfaces of the silicon oxide films are the same, whereby because it becomes possible that a margin of

depth of focus is assured in a photolithographing process when the gate electrode above this surface is patterned, a short-caused by a material of the gate electrode remained at a time of etching the material deposited on the surface of the second silicon oxide film does not occur; it also does not occur that a surface of the semiconductor substrate is etched so as to protrude an etching stopper of the gate oxide film by excessive etching for completely removing the material of the gate electrode.

According to a third aspect of the present invention, there is provided a semiconductor device, further comprising: an inter-layer insulating film having openings reaching the first field effect transistors formed on surfaces of the first field effect transistors, and capacitors connected to the first field effect transistors through the openings, wherein the first gate oxide films are thicker than the second gate oxide films, whereby it becomes possible to form a DRAM having a good refresh property by suppressing leakage currents using the thick gate oxide film and a logic circuit having a high driving capability resulted from the thin gate oxide film and restricting a decrement of a threshold voltage by suppressing an advance narrow channel effect in a single chip.

According to a forth aspect of the present invention, there is provided a method of manufacturing a

semiconductor device, comprising steps of: forming grooves surrounding a first active region and a second active region respectively disposed on a main surface of a semiconductor substrate, forming a first silicon oxide film for embedding the grooves, forming a second silicon oxide film for covering the first active region and the second active region, forming a first mask, having openings on a main surface of the first active region, on a surface of the second silicon oxide film and etching a part of the second silicon oxide film existing on the main surface of the first active region, forming a first gate oxide film on the main surface of the first active region, removing the first mask, forming a second mask, having openings on a main surface of the second active region and etching a part of the second silicon oxide film existing on the main surface of the second active region, removing the second mask, forming a second gate oxide film on the main surfaces of the first and second active regions, and forming first field effect transistors and second field effect transistors on the main surfaces of the first and second active regions, wherein even though the silicon oxide films having different film thicknesses are formed on surfaces of a plurality of active regions in a single chip, the silicon oxide films in the grooves are not dropped along edges of the grooves; and therefore shapes of portions of the active regions in contact with trench isolation can be

formed substantially the same and transistor properties are not affected by the shapes of the active regions.

According to a fifth aspect of the present invention, there is provided a method of manufacturing a semiconductor device, wherein: the first mask is made of a polycrystalline film, whereby the silicon oxide films can be further controllably etched because a selectivity of 50 or more of the polycrystalline film is assured when the silicon oxide films are dry-etched.

According to a sixth aspect of the present invention, there is provided a method of manufacturing a semiconductor device, further comprising steps of: forming an inter-layer insulating film having openings on the inter-layer insulating film, which can reach the first field effect transistors, and forming capacitors which can reach the first field effect transistors through the openings, wherein leakage currents are restricted by making the gate oxide film of the DRAM memory cell thick; it becomes possible to make the shapes of the active region, which drop along the edges of the grooves even though driving capabilities are increased by making the gate oxide film of the other regions thin; and therefore a decrement of a threshold voltage can be restricted by suppressing an inverse narrow channel effect.

According to a seventh aspect of the present invention, there is provided a method of manufacturing a

semiconductor device, further comprising steps of: injecting channels of the first field effect transistors in the first active region before etching the second silicon oxide film on the main surface of the first active region after forming the first mask, and injecting channels of the second field effect transistors in the second active region before etching the second silicon oxide film on the main surface of the second active region after forming the second mask, wherein the channels are injected through the second silicon oxide film; the second silicon oxide film is removed; and the gate oxide film is again formed, whereby it becomes possible to obtain the gate oxide film having an excellent film quality by protecting the surface of the semiconductor substrate at the time of injecting channels.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete application of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanied drawings, wherein:

Figure 1 is a cross-sectional view for schematically showing a part of a semiconductor device according to Embodiment 1 of the present invention;

Figure 2 is a cross-sectional view for schematically

showing a part of the semiconductor device according to Embodiment 1 of the present invention;

Figure 3 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of a method of manufacturing the semiconductor device;

Figure 4 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of a method of manufacturing the semiconductor device;

Figure 5 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 6 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 7 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 8 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 9 is a cross-sectional view for schematically

illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 10 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 11 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 12 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 13 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 14 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 15 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 1 in a step of the method of manufacturing the semiconductor device;

Figure 16 is a cross-sectional view for schematically illustrating a semiconductor device according to Embodiment 2 in a step of a method of manufacturing the semiconductor device;

Figure 17 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 2 in a step of the method of manufacturing the semiconductor device;

Figure 18 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 2 in a step of the method of manufacturing the semiconductor device;

Figure 19 is a cross-sectional view for schematically illustrating the semiconductor device according to Embodiment 2 in a step of the method of manufacturing the semiconductor device;

Figure 20 is a cross-sectional view for schematically showing a part of a conventional semiconductor device;

Figure 21 is a cross-sectional view for schematically showing a part of the conventional semiconductor device;

Figure 22 is a cross-sectional view of a conventional semiconductor device for illustrating a step of a method of producing the device;

Figure 23 is a cross-sectional view of the conventional semiconductor device for illustrating a step

of the method of manufacturing the device;

Figure 24 is a cross-sectional view of the conventional semiconductor device for illustrating a step of the method of manufacturing the device;

Figure 25 is a cross-sectional view of the conventional semiconductor device for illustrating a step of the method of manufacturing the device;

Figure 26 is a cross-sectional view of the conventional semiconductor device for illustrating a step of the method of manufacturing the device; and

Figure 27 is a cross-sectional view of the conventional semiconductor device for illustrating a step of the method of manufacturing the device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A detailed explanation will be given of preferred embodiments of the present invention in reference to Figures 1 through 27 as follows, wherein the same references are used for the same or the similar portions and description of these portions is omitted.

EMBODIMENT 1

Figures 1 and 2 are cross-sectional views of a semiconductor device according to Embodiment 1 of the present invention, wherein Figure 2 is a cross-sectional view taken along a line A-A of Figure 1. In Figure 1, numerical reference 1 designates a semiconductor substrate; numerical reference 2 designates a groove; numerical references 3 and 4 designate silicon oxide

films; numerical references 51 and 52 designate gate oxide films; numerical reference 6 designates a polycrystalline layer; numerical reference 7 designates a metallic silicide layer; numerical reference 8 designates a side wall; numerical reference 9 designates a gate electrode; numerical references 10 through 15 designate source/drain areas; numerical references 61 and 62 designate inter-layer insulating films; numerical references 16 and 23 designate contact holes; numerical reference 17 designates a wire; numerical reference 18 designates a storage node; numerical reference 19 designates a capacitor insulating film; numerical reference 20 designates a cell plate; and numerical reference 22 designates a capacitor. The gate electrode 9 is composed of the polycrystalline layer 6 and the metallic silicide layer 7 such as tungsten silicide, wherein trench isolation is composed of the groove 2, the silicon oxide film 3, and the silicon oxide film 4. The capacitor 22 is composed of the storage node 18 made of polycrystalline silicon containing phosphorus of about 1 through 5 $\times$ $10^{20}/cm^3$, the capacitor insulating film 19 made of silicon oxinitride film having a film thickness of about 5 through 10 nm, and the cell plate 20 made of polycrystalline silicon containing phosphorus of about 1 through 5 $\times$ $10^{20}/cm^3$. The trench isolation is composed of the groove 2, the silicon oxide film 3, and the silicon oxide film 4, which trench isolation separate active

regions.

The wire 17 is connected to the source/drain area 12 through the contact hole 16, and the capacitor 22 is connected to the source/drain area 11 through the contact hole 23. Wires for respectively connecting to the source/drain areas 10 and 13, and the gate electrodes 9 through contact holes, formed in the inter-layer insulating film, are formed (not shown).

In Figure 1, when for example the gate length L_2 of the transistor in the logic circuit as the second field effect transistor is about 200 nm, the width of the groove 2 in the logic circuit is about 200 nm through 500 nm and the depth is about 150 through 500 nm. However, the width of the groove 2 is not unique and may become about 5,000 nm, in such a case by, for example, the semiconductor substrate 1 is left as a dummy pattern in portions without forming the element to adjust the width of the groove 2, whereby an evenness of a surface of the silicon oxide film 4 after embedding can be made small.

The silicon oxide film 3 of about 5 through 30 nm is formed to cover the surface of the semiconductor substrate in the groove 2, and the inside of the groove 2 is embedded by the silicon oxide film 4. On the surface of the semiconductor substrate 1 in the active region of the logic circuit, a gate oxide film 52 of about 4 through 7 nm is formed. The polycrystalline layer 6 of about 50 through 150 nm and the gate electrode 9 made of

the metallic silicide layer 7 having a film thickness of about 50 through 150 nm are formed thereon. In a case that influences of defects in the semiconductor substrate 1 to element properties are sufficiently small, the silicon oxide film 3 can be omitted.

The polycrystalline layer 6 contains phosphorus and arsenic of about $1 \times 10^{21}/cm^3$ in nMOS or boron, boron fluoride and so on of about $1 \times 10^{21}/cm^3$ in pMOS. On the other hand, the source/drain areas 12 and 13 contain phosphorus and arsenic, or boron, boron fluoride and so on respectively of about $1 \times 10^{18}/cm^3$, wherein the source/drain areas is in a lightly doped drain (LDD) structure having a region containing arsenic of about $1 \times 10^{20}/cm^3$ when necessary.

When, for example, the gate length L_1 of the transistor of the DRAM memory cell as the first field effect transistor is about 200 nm, the widths of the grooves 2 is not the same with respect to their locations such that the minimum width is 100 nm through 200 nm and the ordinary width is about 200 nm through 400 nm, and the depths of the grooves 2 are about 150 through 500 nm. Incidentally, the film thicknesses of the gate oxide films are about 7 through 10 nm. Portions not described in the above have a structure similar to that in the logic circuit.

In the DRAM memory cell, information is accumulated by means of electric charges stored in the capacitors;

and a refleshing including reading and writing is conducted at a predetermined period, wherein when leakage currents flow, the information stored in the capacitors is excessively lost to deteriorate a refresh property. Therefore, restriction of leakage currents is important in comparison with transistors in the other portions.

When data are written in the capacitor 22, voltages are applied to electrodes of the memory cell such as V_G=2.0V and V_B=-1.0V, and simultaneously 0V is applied to a bit line (not shown) connected to the source/drain area 10. On the other hand, when data are erased, V_G=2.0V, V_B=-1.0V, and a bit line (not shown) connected to the source/drain area 10 is applied with a voltage of about 2.0V. When the data are read out, a voltage applied to the bit line is about 1.0V.

In the logic circuit, by applying voltages to the gate electrode 9, the source/drain areas 12, 13, and semiconductor substrate 1 (well), a channel is formed in a surface of the semiconductor substrate 1 under the gate electrode 9, wherein one of the source/drain areas 12, 13 is a source and the other is a drain, whereby the logic circuit works as a circuit. When an nMOS transistor is used, voltages to be applied to electrodes of the logic circuit are respectively V_G=2.5V, V_D=2.5V, V_S=0V, and V_B=0V, where references V_G, V_D, V_S, and V_B respectively designate a voltage respectively applied to a gate, a drain, a source, and a semiconductor substrate.

In Embodiment 1, a semiconductor device, in which portions other than the DRAM memory cell has two transistors in these active regions, is used for explanation. However, the present invention is not limited thereto.

According to this semiconductor device, despite formation of a plurality of gate oxide films having different film thicknesses in a single chip, a part of the silicon oxide film 4 along edges of the grooves 2 are not dropped, and shapes of ends of active regions, in contact with trench isolation, can be formed substantially the same, whereby transistor properties are not affected by the shapes of the active regions. Therefore, it is possible to form DRAM having a good refresh property with a small consumption power and high reliability obtained by restriction of a leakage current using a thick gate oxide film and form a logic circuit having a high driving capability using a thin gate oxide film, being a high speed, and having high reliability obtained by restriction of a drop of a threshold voltage as a result of suppression of an inverse narrow channel effect, both in a single chip, whereby miniaturization of the chip is attained maintaining good properties of the semiconductor device.

Further, at portions where the widths of the grooves 2 surrounding these active regions are the same, there is no scattering in the heights of the surfaces of the

silicon oxide films 4 between a position adjacent to an active region formed with the thick gate oxide film 51 and a position adjacent to the active region formed with the thin gate oxide film 52. Thus, it becomes possible to maintain a margin of a depth of focus in a photolithographing process at a time of patterning a gate electrode, and a short does not occur by a remaining gate electrode material left at a time of etching a gate electrode material deposited on the surfaces of the silicon oxide film 4. On the other hand, the surface of the semiconductor substrate is not shaved by excessively etching in order to completely remove the gate electrode material and penetrating the gate oxide film as an etching stopper. Therefore, reliability of the semiconductor device is improved without an incident that leakage currents flow through surface roughness of the semiconductor substrate.

Figures 3 through 14 are cross-sectional views for illustrating steps of a method of manufacturing the semiconductor device according to Embodiment 1 of the present invention. As shown in Figures 8 through 14, a portion in which a thick gate oxide film is formed (hereinbelow, referred to as a thick film portion) and a portion in which thin gate oxide film is formed (hereinbelow, referred to as a thin film portion) are adjacent each other. Hereinbelow, an example that the DRAM memory cell and a sense amplifier are formed in the

thick film portion and the logic circuit is formed in the thin film portion is shown. In Figure 3, numerical reference 21 designates a silicon nitride film; and numerical reference 31 designates a silicon oxide film.

After forming the silicon oxide film 31 having a thickness of about 5 through 30 nm on the semiconductor substrate 1 by thermal oxidation, the silicon nitride film of about 100 through 300 nm is formed. Figure 3 is a cross-sectional view of the semiconductor device after this step.

In the next, anisotropic etching is conducted using a photolithographing pattern (not shown) such as a photoresist formed in portions other than areas for receiving grooves 2. The photolithographing pattern is removed after patterning the silicon nitride film 2. Figure 4 is a cross-sectional view of the semiconductor device after this step.

The silicon oxide film 31 and the semiconductor substrate 1 are subject to anisotropic etching using the remaining silicon nitride film 21 as a mask to form the groove 2 having a depth of 100 through 500 nm on the surface of the semiconductor substrate 1 and the groove 2 having a width of about 100 through 500 nm in the logic circuit. At this time, the width of the groove 2 in the DRAM memory cell is about 100 nm through 200 nm at a portion having the minimum width of isolation and about 200 through 400 nm at portions other than this. Figure 5

is a cross-sectional view for illustrating elements of the semiconductor device after this step.

In the next, the silicon oxide film 4 having a thickness of about 300 nm through 1,000 nm is formed on a whole surface by a low-pressure CVD method; and the silicon oxide film 4 on a surface of the silicon nitride film 21 is removed by a chemical mechanical polishing (CMP) method using the silicon nitride film 21 as a stopper to thereby remain the silicon oxide film 4 only in insides of the openings fabricated by the grooves 2 and the silicon nitride film 21. After removing the silicon nitride film 21 by a wet etching using thermal phosphoric acid, the silicon oxide film 31 is removed. Figure 6 illustrates a cross-sectional view after this step.

In Figure 7, numerical reference 32 designates a silicon oxide film. In the silicon oxide film 32 of about 3 through 15 nm is formed on a surface of the semiconductor substrate 1 by thermal oxidation. Figure 7 is a cross-sectional view for illustrating elements of the semiconductor device after this step. In a case of nMOS, ions such as boron or boron fluoride are implanted over a mask having openings corresponding to nMOS; and in a case of pMOS, ions of impurities such as phosphorus or arsenic are implanted over a mask having openings corresponding to pMOS, wells (not shown) other than channel implantation layers are formed in the DRAM memory

cell and portions other than the DRAM memory cell. This ion-implanting for forming wells can be simultaneously conducted at a time of forming the channel implantation layers, if necessary.

In Figure 8, numerical reference 211 designates a silicon nitride film; and numerical reference 41 designates a resist pattern. After forming the silicon nitride film 211 of about 5 through 30 nm is formed on the silicon oxide film 32, the resist pattern having openings of active regions of the thick-film memory cell, and the silicon nitride film 211 on the surface of the semiconductor substrate 1 of the memory cell is removed using this resist pattern 41. Thereafter, the channel implantation layers (not shown) of the memory cell is formed by implanting ions of boron or boron fluoride. Figure 8 is a cross-sectional view for illustrating the semiconductor device after this step.

In Figure 9, numerical reference 42 designates a resist pattern. The resist pattern 41 is removed; the resist pattern 42 having openings of the active regions of the sense amplifier, which uses transistors having a different threshold voltage from that in the memory cell, is formed in the thick film portion; and the silicon nitride film 211 formed on a surface of the semiconductor substrate 1 of the sense amplifier is removed. Thereafter, a channel implantation layer (not shown) is formed in the active region of the sense amplifier by

implanting ions such as boron. Figure 9 is a cross-sectional view of the semiconductor device after this step. In the thick film portion, when transistors having a further different threshold voltage exist, formation of the resist pattern and implantation of ions may be repeatedly conducted in a similar manner.

In Figure 10, numerical reference 53 designates a silicon oxide film. After removing the resist pattern 42 and the silicon oxide film 32 in the thick film portion by hydrofluoric acid using the silicon nitride film 211 as a mask, thermal oxidation is conducted again to thereby form the gate oxide film 53. Figure 10 is a cross-sectional view of the semiconductor device after this step, in which the gate oxide film 53 is formed in the memory cell and the sense amplifier within a surface of the semiconductor substrate 1, and the silicon oxide film 32 and the silicon nitride film 211 are formed in the logic circuit.

In Figure 11, numerical reference 43 designates a resist pattern. After removing the silicon nitride film 211, the active regions of pMOS of the thick film portion and the thin film portion are covered, and an impurity such as boron and boron fluoride is injected as an ion using a mask of the resist pattern 43, in which the active region of nMOS of the thin film portion is opened, whereby a channel implantation layer (not shown) of nMOS of the logic circuit is formed. In a case of pMOS, in a

manner similar to that in nMOS, the active regions of nMOS of the thick film portion and the thin film portion are covered to form a channel implantation layer (not shown) by injecting ions such as phosphorus and arsenic using a mask, in which the active region of pMOS of the thin film portion is opened. Thereafter, the silicon oxide film 32 is removed. Figure 11 is a cross-sectional view for illustrating the semiconductor device after this step. Although description is made for a case that the threshold voltages of nMOS and pMOS in the logic circuit are respectively one kind, it is necessary to repeatedly inject a channel by separately masking depending on conduction types of channel implantation layers and threshold voltages.

After removing the resist pattern 43, the silicon oxide film 52 having a film thickness of about 4 through 7 nm is formed on a whole surface by thermal oxidation. Figure 12 is a cross-sectional view of the semiconductor device after this step. At this stage, the channel implantation layers are formed in transistors in all areas of the DRAM memory cell, the sense amplifier, and the logic circuit. In Embodiment 1, although the sense amplifier is formed in the thick film portion, it may be formed in the thin film portion. The ions are simultaneously implanted in portions having the same gate oxide film thickness, the same conduction types of the channel implantation layers, and the concentration of

impurities in the channel implantation layers.

In the next, after depositing the polycrystalline layer 6, which contains impurities of about $1 \times 10^{21}/cm^3$, such as phosphorus and arsenic in a case of nMOS, and boron and boron fluoride in a case of pMOS and has a film thickness of about 50 through 100 nm, by a CVD method and forming a metal silicide layer 7 such as tungsten silicide by a CVD method or a sputtering method, a gate electrode 9 is formed by patterning.

Source/drain areas 10 through 15 are formed by injecting ions of about $3 \times 10^{13}/cm^2$ of phosphorus or arsenic in nMOS or of boron or boron fluoride in pMOS under about 20 through 40 keV; and side walls 8 are formed by depositing and etching-back the silicon oxide film by about 50 through 100 nm using a low pressure CVD method. Figure 13 is a cross-sectional view for illustrating the semiconductor device after this step. When the source/drain areas 12 through 15 are made to be a lightly doped drain (LDD) structure, portions receiving the memory cell is covered by a mask, and the source/drain areas (not shown) include impurity regions having a concentration of impurities of about $1 \times 10^{20}/cm^3$ formed by implanting arsenic in nMOS or boron or boron fluoride in pMOS.

Thereafter, an inter-layer insulating film 61 of about 200 through 600 nm is deposited by a low-pressure CVD method, and a contact hole 16 reachable the

source/drain area 12 is opened to have a diameter between 0.1 μm through 0.5 μm by a dry etching method. After depositing a polycrystalline silicon of about 50 through 150 nm containing phosphorus of about 1×10^{20} through $5 \times 10^{20}/cm^3$ by a CVD method, tungsten silicide (WSi) of 50 through 150 nm is deposited by a CVD method and patterned to form a wire 17. Figure 14 is a cross-sectional view for illustrating the semiconductor device after this step.

Further, after forming an inter-layer insulating film (not shown), contact holes (not shown) are formed; and a wire material is embedded in the contact holes, whereby a wire connected to the source/drain area 10 (bit line) and wires connected to the source/drain areas 13 through 15 are formed (not shown). Wires connected to the source/drain areas 10, and 12 through 15 can be formed in any order for the convenience of a circuit structure.

After forming an inter-layer insulating film 62 and a contact hole 23, polycrystalline silicon of about 600 through 1,000 nm containing an impurity such as phosphorus of about 1×10^{20} through $5 \times 10^{20}/cm^3$ is deposited on a whole surface and is arranged at a predetermined area by patterning, whereby a storage node 18 is formed. Thereafter, by depositing a silicon oxynitride film of about 5 through 10 nm, to be a capacitor insulating film 19, is deposited by a CVD method, and by depositing and patterning polycrystalline

silicon of about 50 through 100 nm containing an impurity such as phosphorus of about 1×10^{20} through $5 \times 10^{20}/cm^3$, to be a cell plate 20, a capacitor 22 is formed. As described, the semiconductor device shown in Figure 1 is formed.

Further, at the step that the contact holes reachable to the source/drain areas 10 through 15 are formed, areas of impurities having the same conduction types as the source/drain areas exposed to the contact holes can be formed by injecting self aligned contact (SAC). Such areas of impurities are formed by injecting phosphorus of 1×10^{13} through $1 \times 10^{14}/cm^2$ under 50 through 150 keV so as to have a concentration of impurities of about $1 \times 10^{18}/cm^3$, whereby it becomes possible to relax an electric field of a p-n junction caused by a peak of a concentration of impurities between the channel implantation layer and the source/drain areas and to restrict leakage currents from the capacitor 22 to the semiconductor substrate 1 (well), whereby a refresh property becomes satisfactory and reliability of the semiconductor device is improved. Further, in portions other than memory cell, by injecting ions of about 5×10^{13} through $30 \times 10^{13}/cm^2$, i.e. phosphorus in nMOS, and boron or boron fluoride in pMOS, under 20 through 50 keV to make areas of impurity having a concentration of impurities of about $5 \times 10^{18}/cm^3$, it becomes possible to

reduce contact resistances between wires embedded in the contact holes and the source/drain areas; and a driving capability is improved.

Although, in Embodiment 1, the semiconductor device in which the logic circuit, the DRAM memory cell, and the sense amplifier are formed, is described, the present invention is not specifically limited thereto as long as a plurality of thicknesses of gate oxide films are used in a single chip.

In accordance with the method of manufacturing this semiconductor device, since the number and the conditions for removing the silicon oxide films formed on the surface of the active region are substantially equal in the step of forming the plurality of gate oxide films having different film thicknesses in the single chip, the portion of the silicon oxide film 4 along the edge of the groove 2 is not dropped. Accordingly, even though the gate oxide films having different film thicknesses are formed on the surface, it becomes possible to form the portion of the active region in contact with the trench isolation substantially the same, and the properties of the transistor are not affected by the shape of the active region. Therefore, transistor properties are not affected by the shapes of the active region. Thus, it is possible to obtain the method of manufacturing the semiconductor device miniaturized maintaining the desirable semiconductor device properties, in which the

DRAM memory cell with improved refresh characteristics, a low consumption power, and improved reliability by restricting leakage currents using the thick gate oxide film and the logic circuit with an improved driving capability, a high speed, and improved reliability which can restrict a drop of the threshold voltage by suppressing an inverse narrow channel effect using the thin gate oxide film.

Further, since the number and the conditions for etching the surfaces of the silicon oxide film 4 are the same in both of the portion adjacent to the active region having the thick gate oxide film and the portion adjacent to the active region having the thin gate oxide film, there is no scattering in the heights of the surfaces of the silicon oxide films 4 in grooves 2 having the same widths. Thus, it is possible to assure a margin with respect to a depth of focus in the photolithographing process at the time of patterning the gate electrode, and a short caused by the gate electrode material remained at a time of etching the material deposited on the surfaces of the silicon oxide films 4 does not occur. On the other hand, since the surface of the semiconductor substrate is not shaved as long as an excessive etching for completely remove the gate electrode material is not conducted and the gate oxide film having an etching stopper is not penetrated, an yield is improved, and reliability is improved without a danger of generating

leakage currents caused by a rough surface of the semiconductor substrate.

In Figure 15, numerical reference 212 designates a polycrystalline film. After forming the trench isolation on the surface of the semiconductor substrate, the silicon oxide film 32 is formed on the surface; and the polycrystalline film 212 is formed thereon. Figure 15 is a cross-sectional view for illustrating the semiconductor device at this stage. The polycrystalline film 212 is formed instead of the silicon nitride film 211 as a mask for etching the silicon oxide film 32. The order of removing the silicon oxide film 32 using a plurality of resist patterns is similar to that in the silicon nitride film 211. Removal of this polycrystalline film is conducted by an isotropic dry etching. Although the selectivity of the silicon nitride film is about 3 through 20 at a time of dry-etching the silicon oxide film 32, because the selectivity of the polycrystalline film is assured to be 50 or more, it is possible to controllably etch the silicon oxide film 32 and it is effective for microminiaturizing the semiconductor device.

EMBODIMENT 2

Figures 16 through 18 are cross-sectional views for illustrating steps of the method of manufacturing the semiconductor device according to Embodiment 2 of the present invention, wherein Embodiment 2 is another method of manufacturing the semiconductor device described in

Embodiment 1. According to the method of manufacturing, the semiconductor device shown in Figure 1 can be manufactured.

In a similar manner to Embodiment 1, trench isolation composed of a groove 2 and silicon oxide films 3 and 4 is formed on a surface of a semiconductor substrate. A silicon oxide film 32 is formed in a similar manner to Embodiment 1; boron or boron fluoride are implanted as an ion after forming a mask, in which a portion corresponding to nMOS is opened; and an impurity such as phosphorus or arsenic is implanted as an ion after forming a mask, in which a portion corresponding to pMOS is opened, to thereby form a well (not shown) other than channel implantation layer in a memory cell and portions other than this. These steps are the same as those in Embodiment 1.

In Figure 16, numerical reference 44 designates a resist pattern. After forming a silicon nitride film 211 of 5 through 30 nm on the silicon oxide film 32 in a similar manner to Embodiment 1, a resist pattern 44 for covering a thin film portion is formed, and the silicon nitride film 211 on the surface of the semiconductor substrate 1 in a thick film portion is removed using this resist pattern 44. Figure 16 is a cross-sectional view for illustrating the semiconductor device after this step. Even though, in Embodiment 1, the channel implantation layer is formed and the silicon nitride film 211 is

simultaneously removed with respect to portions having different threshold voltages such as the memory cell and the sense amplifier when the portions have the same thicknesses of gate oxide films, the silicon nitride film 211 is removed with respect to portions having the same thicknesses of the gate oxide films.

In the next, after removing the resist pattern 44, a resist pattern 41, in which an active region of the memory cell is opened, is formed, and a channel implantation layer (not shown) of the memory cell is formed by implanting boron or boron fluoride as an ion. Figure 17 is a cross-sectional view of the semiconductor device after this step.

After removing the resist pattern 41, a resist pattern 42, in which an active region of the sense amplifier is opened, is formed, and the channel implantation layer (not shown) of the sense amplifier is formed by implanting ions. Figure 18 is a cross-sectional view for illustrating the semiconductor device after this step. Similarly to Embodiment 1, when transistors having further different threshold voltages exist in the thick film portion, formation of a resist pattern and ion-implantation are similarly repeated.

In the next, in a similar manner to Embodiment 1, after removing the resist pattern 42, the silicon oxide film 32 on the surface of the semiconductor substrate in the thick film portion is removed using the silicon

nitride film 211 as a mask and thereafter a silicon oxide film 53 is again formed by thermal oxidation. After removing the silicon oxide film 32 remaining in the surface of the semiconductor substrate in the logic circuit in a similar manner to Embodiment 1, the silicon oxide film 52 having a film thickness of about 4 through 7 nm is formed on a whole surface by thermal oxidation. Similarly to Embodiment 1, a gate electrode 9, source/drain areas 10 through 13, a side wall 8, an inter-layer insulating film 61, a wire 17, an inter-layer insulating film 62 and a capacitor 22 are formed. As described, the semiconductor device shown in Figure 1 is formed.

According to a method of manufacturing the semiconductor device of the present invention, because the number and the conditions of removing the silicon oxide film formed on these surfaces of the active regions are made substantially the same in the step of forming the plurality of gate oxide films having different thicknesses in the single chip, the portions of the silicon oxide film 4 along the edge of the grooves 2 are not dropped. Accordingly, even though the gate oxide films having different thicknesses are formed on the surface, it is possible to make shapes of portions of the active regions in contact with the trench isolation substantially the same, whereby transistor properties are not affected by the shapes of the active regions. Thus,

it is possible to form a DRAM memory cell having improved refresh properties, a low consumption power, and improved reliability by suppressing leakage currents using the thick gate oxide film and a logic circuit, in which a driving capability is improved, a drop of the threshold voltage can be restricted by suppressing an inverse narrow channel effect, a high speed and improved reliability are obtainable using the thin gate oxide film, in the single chip, whereby the method of manufacturing the semiconductor device miniaturized maintaining desirable properties of the device is obtainable.

Further, since the number and the conditions of etching the surface of the silicon oxide film 4 is the same with respect to portions adjacent to active regions having the thick gate oxide film and portions adjacent to active regions having the thin gate oxide film, the heights of the surfaces of the silicon oxide films 4 are not scattered as long as the widths of the grooves 2 are equal. Thus, it is possible to assure a margin of a depth of focus in a photolithographing process at a time of patterning the gate electrode, a short, caused by a gate electrode material remaining at a time of etching the gate electrode material deposited on the surface of the silicon oxide film 4, does not occur. On the other hand, the surface of the semiconductor substrate is not shaved because an etching for completely removing the gate electrode material is not excessively conducted and

the gate oxide film as an etching stopper is not penetrated, whereby an yield is improved; and there is no danger that leakage currents are generated by surface roughness of the semiconductor substrate, wherein the semiconductor device having improved reliability is obtainable.

Further, according to the method of manufacturing the semiconductor device described in Embodiment 1, it may occur that an end portion of the silicon nitride film 211 is covered above the trench isolation located between the sense amplifier and the memory cell at a time of forming the resist pattern 42 having openings above the sense amplifier as shown in Figure 19; and the silicon nitride film 211 is left without being etched in the end portion. When the silicon nitride film 211 is left, the silicon oxide film 32 therebelow is not etched; and the gate oxide film 53 is not formed by thermal oxidation, whereby the silicon oxide film 32 is left as a gate oxide film at this part. In this case, a dielectric breakdown of the gate oxide film may occur because a quality of film is deteriorated after various steps such as ion-implanting for forming a well. On the contrary, according to the method of manufacturing the semiconductor device described in Embodiment 2, when the silicon nitride film 211 used as a mask for determining the thicknesses of the gate oxide films 51 and 52 is removed after removing the whole silicon nitride film 211

in the thick film portion by the resist pattern 44, requisite treatment such as channel implantation is conducted; and the remaining silicon nitride film 211 is selectively removed by hot phosphoric acid or the like. By such a method, because the silicon nitride film 211 is not left by a deviation of the resist pattern, an yield is improved by maintaining a margin of the resist pattern.

Similarly to Embodiment 1, when the polycrystalline film is used instead of the silicon nitride film 211, because the selectivity of the polycrystalline film is higher than that of the silicon nitride film in dry-etching the silicon oxide film 32, it is possible to more controllably etch the silicon oxide film 32, whereby microminiaturization of the semiconductor device can be effectively conducted.

The first advantage of a semiconductor device according to the present invention is that miniaturization of a chip is attainable keeping properties of elements respectively formed in a thick film portion and a thin film portion of gate oxide films desirable.

The second advantage of the semiconductor device according to the present invention is that a short caused by a remaining gate electrode material at a time of etching the material deposited on a surface of a silicon oxide film does not occur, and reliability of the device is improved without a danger of generating leakage

currents caused by surface roughness of a semiconductor substrate.

The third advantage of the semiconductor device according to the present invention is that miniaturization of a chip is attainable by maintaining properties of the semiconductor device desirable.

The forth advantage of a method of manufacturing the semiconductor device according to the present invention is that the semiconductor device having a miniaturized chip is obtainable maintaining properties of elements respectively formed in the thick film portion and the thin film portion of the gate oxide films desirable.

The fifth advantage of the method of manufacturing the semiconductor device according to the present invention is that the microminiaturizing semiconductor device is obtainable using a polycrystalline film as a mask for etching a second silicon oxide film.

The sixth advantage of the method of manufacturing the semiconductor device according to the present invention is that the miniaturized semiconductor device is obtainable while maintaining properties of the semiconductor device desirable.

The seventh advantage of the method of producing the semiconductor device according to the present invention is that the semiconductor device having high reliability is obtainable by protecting a surface of the semiconductor substrate by injecting channels of the

elements through the second silicon oxide film.

Obviously, numerous modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described herein.